ABSTRACT

In an insulated gate semiconductor device (1) having an N⁻ type base region (11), P⁺ type collector regions (12), P type base regions (13), and N⁺ type emitter regions (14), an N⁺ type collector-short region (15) which extends toward the N⁻ type base region (11) farther than the P⁺ type collector regions (12) is formed in the lower surface of the N⁻ type base region (11), and a P⁺ type semiconductor region (16) is formed between the N⁺ type collector-short region (15) and the N⁻ type base region (11).